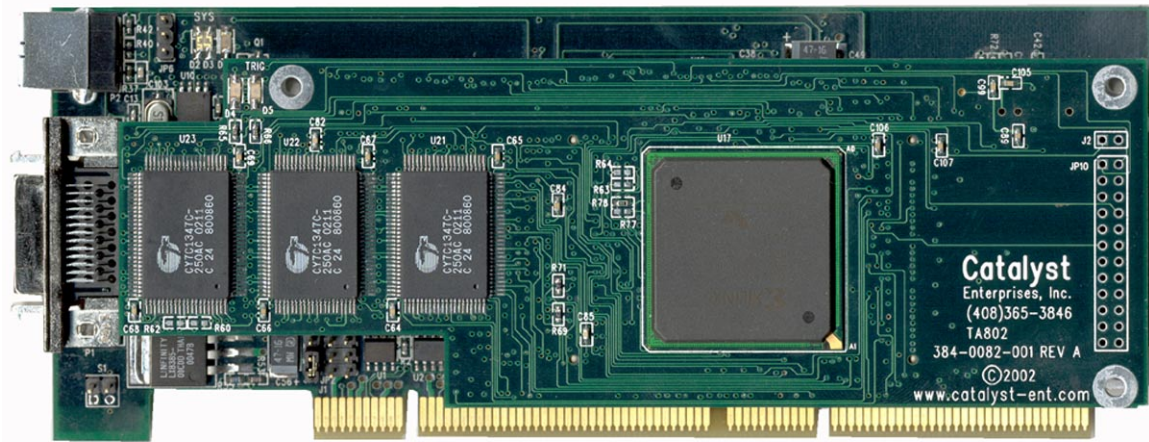


133 MHz PCI-X - PCI Analyzer & Exerciser



- ◆ 133 MHz, PCI-X Analyzer/Exerciser
- ◆ 66 MHz, PCI Analyzer/Exerciser
- ◆ Master or target mode, Transparent or PCI-X/PCI agent
- ◆ Ultimate Dual-mode GUI Interface optimized to enhance product development
- ◆ Interactive “Linked” Analyzer/Exerciser – 64 Bit, 133 MHz
- ◆ Giga Bytes/Sec real-time continuous Performance Analysis & traffic generation
- ◆ Automated PCI Device Compliance Test & Verification
- ◆ C-API for custom C program development
- ◆ FPGA design automatically upgrades the product features with each software update

PCI-X / PCI, TARGET SYSTEM

Analyze any 3.3V PCI-X or PCI System Architecture running under any operating system.

AUTOMATIC SYSTEM CLOCK DETECTION & REPORTING

The TA800 automatically detects and reports the system clock frequency.

FIELD UPGRADEABLE

FPGA based design allows automatic hardware upgrade to the latest added features each time a new version of the software is loaded.

VOLTAGE CHECK

You may enable the TA800 to monitor the system voltages for a drop exceeding 5% of nominal and to flag this by illuminating a red LED.

HOST SOFTWARE

The TA800 software operates under Windows XP, 2000, NT SP 3.1 or higher, 98 or 95.

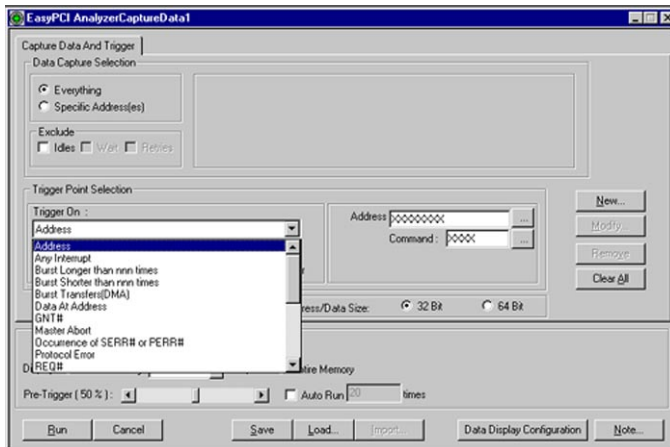
Easy Mode (PRE-DEFINED)

PRE-DEFINED SETUPS ALLOW INSTANT DEBUG & ANALYSIS OF HARDWARE AND SOFTWARE PROBLEMS

“Capture Data & Trigger” mode allows hardware or software oriented PCI-X/PCI bus debug, without requiring any programming or setup of the analyzer. A comprehensive selection of Pre-Defined setups allows capturing data on variety of trigger selections.

In addition to the pre-defined setups for data capture and trigger of bus cycles there are also several selections available for performance analysis, statistical analysis and TA800 as a bus Master to read and write variety of target registers and memory contents.

Capture Data & Trigger menu allows users to easily select capturing everything or to exclude Idles, Waits and Retries and/or to capture data at a specific address range. At the same time the user may also specify the trigger point from variety of available selections.



There are several selections available for triggering on an occurrence of a single signal to triggering on events causing system crashes

PRE-DEFINED PCI-X PROJECTS FOR "DATA CAPTURE & TRIGGER" MODE

- Trigger on specified address.
- Trigger on any interrupt.
- Trigger on a specific attribute phase.
- Trigger on burst longer than nnn times.

- Trigger on burst shorter than nnn times.
- Trigger when data burst is transferred.
- Trigger on specified data at address.
- Trigger when GNT# is asserted.
- Trigger when master abort occurs.
- Trigger on SERR# or PERR#.
- Trigger when a PCI-X protocol error is detected.
- Trigger when REQ# is asserted.
- Trigger when reset is de-asserted at rising edge of reset.
- Trigger when signal xxx is asserted and then de-asserted nnn times.
- Trigger when signal xxx asserted for more than nnn times.
- Trigger when signal xxx de-asserted and then asserted for nnn times.
- Trigger when signal xxx de-asserted for more than nnn times.
- Trigger when signal xxx is shorter than nnn times.
- Trigger on a target abort.
- Trigger on a target disconnect.
- Trigger on a target Retry.
- Trigger on target disconnect termination.
- Trigger on target disconnect during burst.
- Trigger on Vendor ID and Device ID.

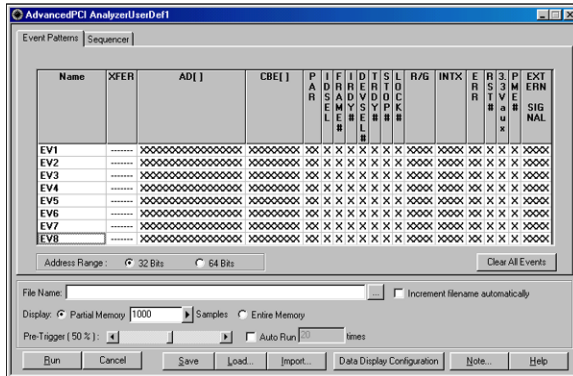
Advanced Mode (USER SETUP) FOR DEBUGGING OF MORE COMPLEX PROBLEMS

Users may define up to eight events covering all PCI bus signals for data/address capture or triggering. In addition the external signals may also be defined in the event menu for a condition on jump or trigger.

Up to 16 level states may be defined in the Sequencer. At each state the user may define what to capture and where to jump depending on occurrences of events and/or their Boolean expression and protocol errors. Unlimited Else If and jumps may be defined in the Sequencer menu.

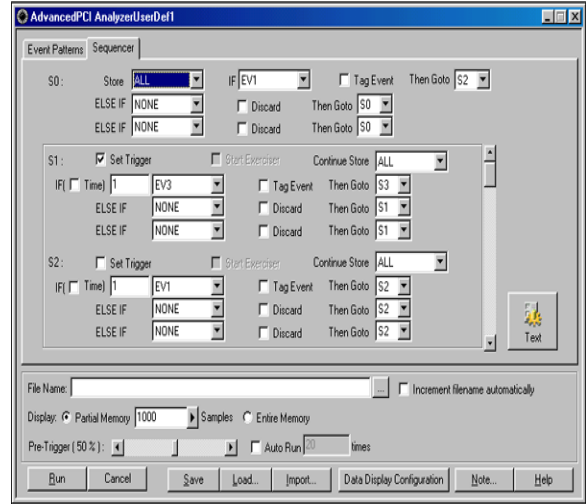
The advanced mode requires Event, Sequencer and Program files (for the exerciser mode) to be defined by the user.

Some examples of the Events and Sequencer features are indicated below.

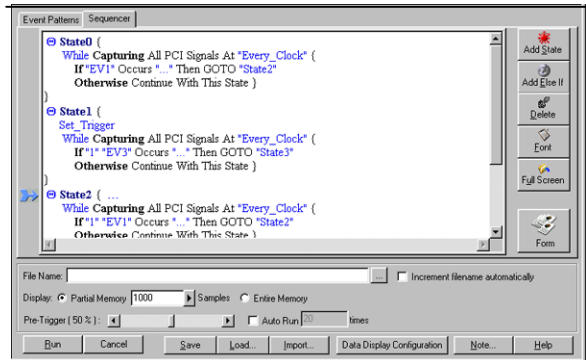


The user defined menu also allows users to specify the output file name, pre-trigger value, number of data to be captured, notes about the setup by the user and execution of the program from the menu.

The Sequencer may be programmed using either, an intuitive GUI or a convenient textual programming window.



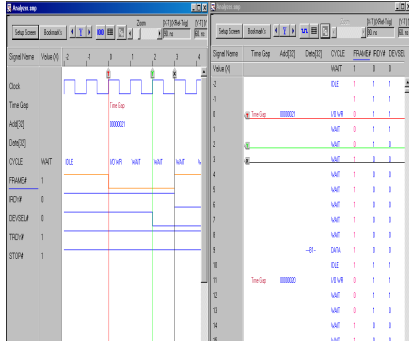
Sequencer, Menu style



Sequencer, Text style

DISPLAY CAPABILITY

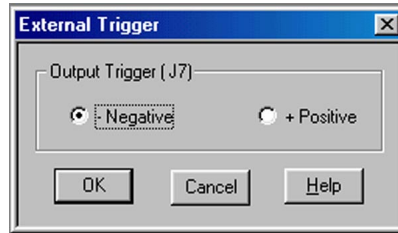
- List or Waveform display of captured data, displayed individually or simultaneously.



- Ability to add/remove and rearrange captured signals by dragging signal names in the display windows.
- Display the value of X or Y cursor position.
- User defined color for each signal.
- Indicating "Time Gap" for when data discontinuity exist.
- User defined "Bookmark".
- Graphical display of latency time.
- Three waveform display cursors with their relative positions expressed as time or clocks.
- Cursors linked between waveform and list windows.
- Waveform display zoom from 0.1 to 10 about X, Y or around X and Y cursors.
- Jump relative to Trigger, X, Y Cursor or start within waveform display.
- Any of PCI signals may be added or removed from the screen.

EXTERNAL OUTPUT TRIGGER

A positive or negative level may be set for the external trigger output, external trigger will get set when trigger occurs in the sequencer.



REVIEW AND EDIT FILES IN OTHER FORMATS

Output files may be converted to ASCII text or EXCEL™ spreadsheets for use in off-line data analysis programs. Also available from the tools menu is a graphical screen capture to a *.PCX file format.

POST PROCESSING UTILITIES

SEARCH UTILITY

The search utility offers you the capability to:

- Search for any pattern.
- Search for consecutively recurring patterns.
- Search forward or backward.
- Search for patterns with user defined mnemonics.

COMPARE UTILITY

Allows the comparison of two captured files, entire file or partial.

DATA FILTERING

You may filter captured data files to include or exclude data patterns defined in mnemonics.

MNEMONICS

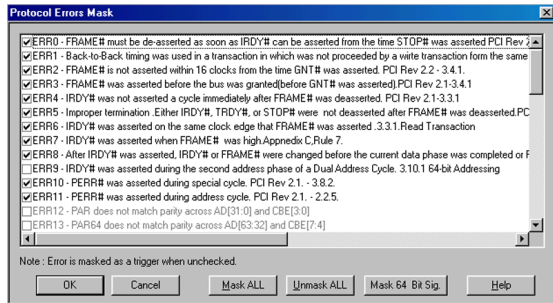
Up to 100 mnemonics may be assigned to 100 different patterns and saved as a file. An unlimited number of mnemonic files may be designed for use in various applications.

Mnemonics may be used to:

- Distinguish certain patterns in the display by name.
- Filter a pattern in or out of a data file.
- Search for patterns by name.

PCI-X PROTOCOL ERRORS

The TA800 monitors and captures over 50 PCI-X/PCI protocol errors automatically whenever a data capture occurs. All or any of the protocol errors may be set to initiate a trigger by using a Protocol Error mask when the protocol error selection is chosen from the "Trigger On" menu in the sequencer.

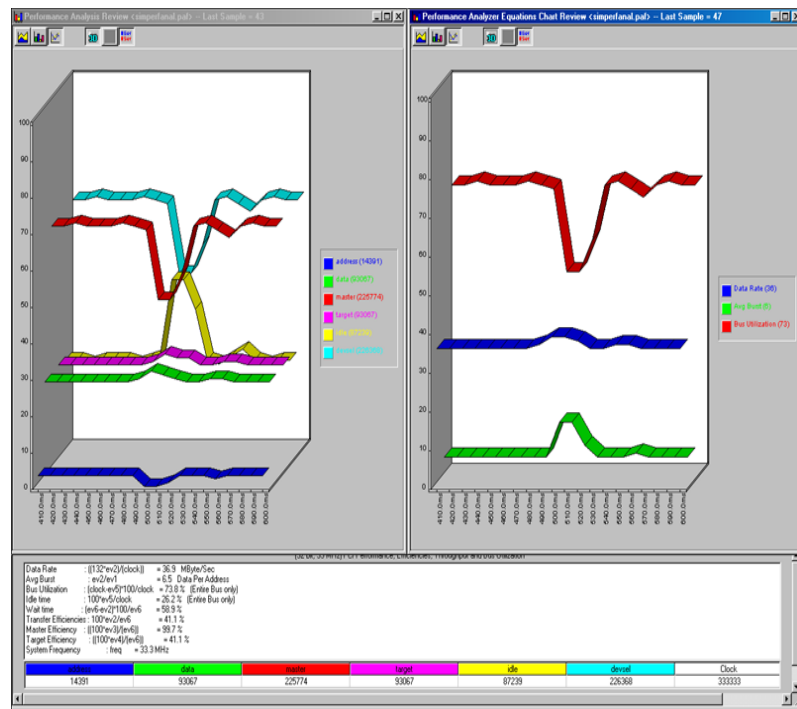


CONTINUOUS REAL TIME PERFORMANCE ANALYSIS

The TA800 real time Performance Analysis is designed with dual ported FIFOs to interface between the hardware and the host. This allows the counting of events in true real time and provides the user with a complete and accurate measurement up to 796 Mb/sec.

- 12 event counters, 8 for monitoring PCI bus other 4 for external signals.
- Users may use the provided setups to measure the most typical parameters or design their own.
- Count actual data transfers for any agent or agents matching user specified address.

- Count DMA transfers for a specific agent or the entire bus.
- Measure and report bus utilization efficiencies, throughput, latencies and retries.
- Report intervals selectable from 500 μ sec to 10 minutes.
- Eight color display
- Record the analysis in graphical format for later review or demonstration of your product performance without having your hardware present.
- Performance Analysis can work simultaneously with the exerciser to generate traffic on the bus and measure performance of the target.

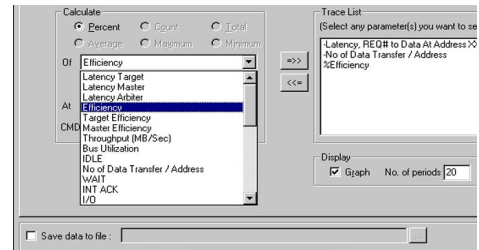


STATISTICAL ANALYSIS

Statistical Analysis is implemented by capturing data in memory and then performing software post processing.

Statistical Analysis measures and reports on Min, Max and Average occurrences for several different parameters such as Latencies, Retry, Data Transfers, Command Utilization, Bus Utilization and various Target Terminations.

The data capture for post processing may be initiated per user defined events on the bus, yielding a repetitive and consistent result.



The parameters measured may be selected for graphical display on the screen and may be saved as graphical or list files for later review.

In the exerciser mode the TA800 can interrogate a target while the trace statistics measures the latency response.

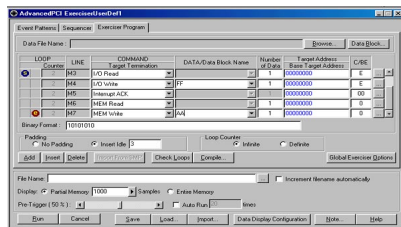
EXERCISER

The 133 MHz 64 bit exerciser operates as Master and Target.

On board target memory allows testing read/write operation of master agents. This option is to be added in the SW version 4.3 and higher.

PROPRIETARY ENGINE:

- Emulates special bus cycles.
- Force errors.
- Inserts Wait states.
- Allows infinite looping on test programs such as DMA read write to saturate the bus.
- Allows conditional start of the exerciser as a Master or as a Target defined in the sequencer.
- Allows forced interrupts within a program for specified number of clocks or continuously outside the test program until reset by user.
- Allows definition and execution of non-compliant PCI protocols and patterns to test the response of other agents on the bus.
- Generates arbitrary patterns for worst case bus traffic.



- All the above operations may be performed by the convenient GUI or a Text Editor.

PRE-DEFINED MASTER PCI COMMANDS

- Interrupt Acknowledge
- Special Cycle
- I/O Read
- I/O Write
- MEM Read DWORD

- MEM Write
- Memory Read Block (Alias)
- Memory Write Block (Alias)
- Configuration Read
- Configuration Write
- Split Completion
- Memory Read Block
- Memory Write Block
- Dual Address I/O Read
- Dual Address I/O Write
- Dual Address Mem Read DWORD
- Dual Address Mem Write
- Dual Split Completion
- Dual Address Mem Read Block (Alias)
- Dual Address Mem Write Block (Alias)
- Dual Address Mem Read Block
- Dual Address Mem Write Block
- Target
- Target Single Data Phase
- Target Disconnect at Next ADB
- Target Retry
- Target Abort
- Target Split Response
- NOP

PRE-DEFINED MASTER PCI COMMANDS

- Interrupt Acknowledge
- Special Cycle
- I/O Read
- I/O Write
- Memory Read
- Memory Write
- Config Read
- Config Write
- MEM Read Multiple
- MEM Read Line
- MW & Invalidate
- DAC: I/O Read
- DAC: I/O Write

- DAC: MEM Read
- DAC: MEM Write
- DAC: MEM Read Multi
- DAC: MEM Read Line
- DAC: MW & Invalidate

PCI TARGET TERMINATION COMMANDS

- Data Transfer
- Disconnect with data
- Disconnect without data
- Target Abort with data
- Target Abort without data
- Retry

SIMPLE PROGRAMMING

Create custom exerciser test programs with simple input program GUIs or import ASCII compatible input program files. Any combination of Master or Target commands (not at the same time) with the corresponding data files (Up to 128K deep) can be composed as an exerciser to be executed once or in a loop.

GENERATE DATA FILES

Create custom exerciser data files manually or take advantage of automatic generation of walking 0 or walking 1 shift right or shift left patterns up to 128K deep.

EXERCISER UTILITIES

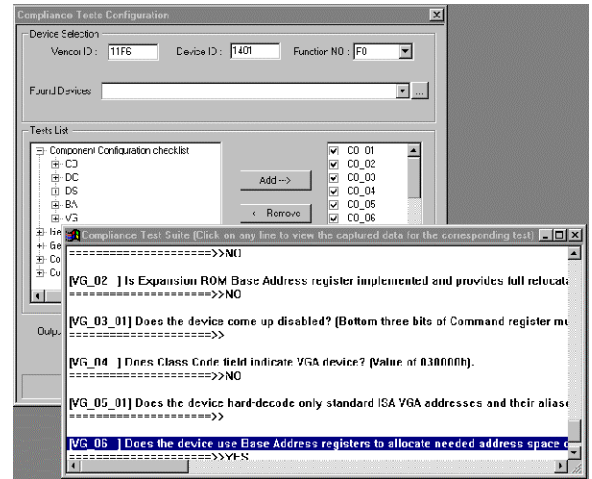
- Perform a memory dump from a specified address to a specified end address or specify the count of data to be dumped.
- Read the contents of an address, modify it and write back to that address.
- Write/read back and verify a block of data in a single or burst mode for an I/O, memory or config target address.
- Scan Configuration Registers finds all PCI agents on the local and the secondary bus.

PCI COMPLIANCE DEVICE TEST

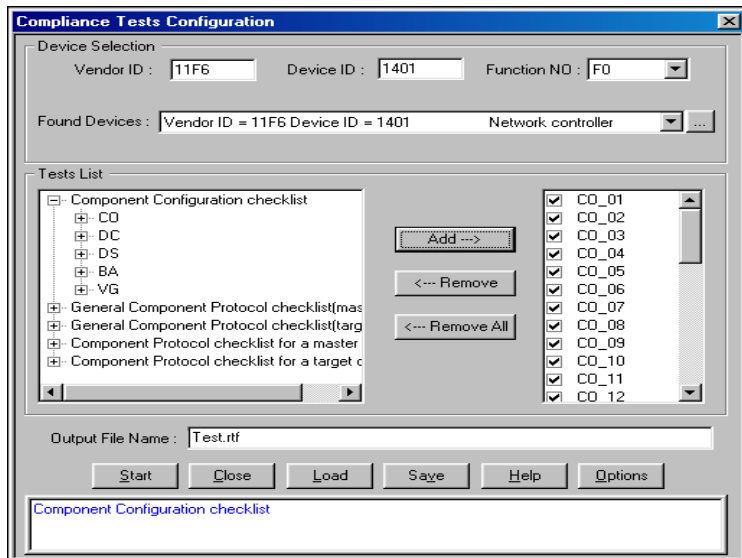
Built in comprehensive compliance device test performs the **PCI Compliance Checklist Verification** on the desired PCI device.

This test performs Device Compliance Check in accordance with the component configuration checklist and generates a comprehensive report matching the PCISIG document with marked responses to each test. Sections of the verifications included are:

- Component Configuration Checklist (CO, DC, DS, BS, BA, VG)
- General component protocol (Master)
- General component protocol (Target)
- Component protocol check for a Master device.
- Component protocol check for a Target device



Screen Test results



Device Compliance Test Selection Menu

In addition, the data captured for each of the tests may be viewed by simply clicking the mouse pointer on the generated report and the captured data will be displayed on the screen.

Component Configuration Checklist		
Test	Description	Result
CO_01	Does each PCI resource have a configuration space based on the 256 byte template defined in section 6.1, with a predefined 64 byte header and a 192 byte device specific region?	Yes ✓ No N/A
CO_02	Do all functions in the device support the Vendor ID, Device ID, Command, Status, Header Type and Class Code fields in the header? See figure 6-1.	Yes ✓ No N/A
CO_03	Is the configuration space available for access at all times?	Yes ✓ No N/A
CO_04	Are writes to reserved registers or read only bits completed normally and the data discard?	Yes ✓ No N/A
CO_05	Are reads to reserved or unimplemented registers, or bits, completed normally and a data value of 0 returned?	Yes ✓ No N/A
CO_06	Is the Vendor ID a number allocated by the PCI SIG?	Yes ✓ No N/A
CO_07	Does the Header Type field have a valid encoding?	Yes ✓ No N/A
CO_08	Do multi-byte transactions access the appropriate registers and are the registers in "little endian" order?	Yes ✓ No N/A
CO_09	Are all READ ONLY register values within legal ranges? For example, the interrupt pin register must only contain values 0-4.	Yes ✓ No N/A
CO_09	Latency Timer Implementation .	OK
CO_09	Interrupt Line Implementation .	OK
CO_10	Is the class code in compliance with the definition in Appendix D?	Yes ✓ No N/A
CO_10	Base Class is :	Network controller
CO_10	SubBase Class is :	Ethernet controller
CO_11	Is the predefined header portion of configuration space accessible as bytes, words, and dwords?	Yes ✓ No N/A
CO_12	Is the device a multifunction device?	Yes No ✓ N/A
CO_13	If the device is multifunction, are configuration space accesses to unimplemented function ignored.	Yes No N/A ✓

Final Test Results

TA800 COM API

A COM Object library included with your analyzer enables programmers to incorporate most of the TA800 functionality in their own programs developed on platforms such as Microsoft Visual C++, Borland Delphi and Microsoft Visual Basic.

The major components are:

- ◆ A project server interface that allows the user to run a predefined project.

 - ◆ A change project server interface that allows the user to modify a predefined TA800 project.

 - ◆ A utility server that allows the user to collect information from the TA800 board.
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SPECIFICATIONS

ANALYZER

Bus Type	
TA800	PCI – PCI-X, 3.3V Key
Bus width	32 or 64 bit wide
Maximum Clock Rate	Up to 133MHz PCI-X Up to 66 MHz, PCI
Min	1 KHz
1 External Trigger Out	Positive or negative TTL Level synchronized to the sequencer first time trigger.
Memory Depth per Channel	
Trace, 95 PCI signals	128K
Trace, optional	4 Meg (Not available at this time)
Exerciser, 95 signals	128K
Protocol Errors	128K
Time Tag	128K
Word Recognizers	8 Event patterns.
Triggering Events	Any of the 8 events, Boolean equation of the events, external input channels or trigger on timing or protocol errors.
14 - 20 bit Counters	Used as 30 event or delay counters at each state.
16 Level Sequencer	Supported at each level by Store, Set Trigger, Set Tag, Discard, If, Else If, GoTo, Delay Time, Delay Count and Start Exerciser statements.
Counter Use	Count Accumulative Count & reset as High Pass filter for triggering on system crashes.

Count & reset as Low Pass filter.

TIME TAG

Counter	40 bits
Resolution	15 ns to 40 ns
Recording Duration	up to 5 Hours at 15 ns, up to 10 Hours at 30 ns.
Reported display	Absolute time from the start, Relative to trigger point, relative to each data sample, Latencies for Target and Master.

PERFORMANCE ANALYSIS

Real-time, Continuous

Event Counters	8 32 bit counters.
Count qualifier	Every bus cycle, User defined address space or Sequencer (Based on user defined sequence of events)
Count Modes	Reset or Accumulative
Count Interval	500 us to 10 minutes
Output Results Reports	
Pre-defined	Bus utilization, Efficiencies, Throughput, Latencies, DMA transfers, Idle time; I/O vs. Memory utilization.
Custom	Per user defined equations.
Measurement Reports	Normalized to largest per interval or Absolute measurement.
Output Display (real Time)	Text Report, Bar Graph, Pie Chart and histogram.
Display Modes	Color; 2D or 3D
Host CPU interface	Real-time FIFOs

Statistical (Memory Capture)

Capture Depth	User defined up to 128 K
Capture Qualifier	User defined sequence of events.
Measurement types	Min, Max or Average. Number of occurrences. Percentage of occurrences.
Measurement Qualifiers	User-defined address, address range or cycle type.
Report Types	Graphical and Text

Measured Parameters

Latency Target
Latency Master
Latency Arbiter
Efficiency
Target Efficiency
Master Efficiency
Throughput Mb/Sec
Bus Utilization
IDLE
No of Data Transfer/Address
Wait
Int Ack
I/O
I/O RD
I/O WR
Memory
Mem RD
Mem WR
Configuration
CFG RD
CFG WR
MEM RM
Dual ADD
MEM RL
MEM W&I
Total No of Data
RETRY
TABORT
DIS+DATA
DIS-DATA
MABORT
Latency, REQ# to Data

UTILITIES

Search	By name, forward, backward and for consecutively re-occurring patterns.
Post-capture filter	Include or exclude user defined patterns.
Convert Captured Data	ASCII EXCEL PCX
Compare Captured Data	User defined start and end from each file.
Jump Within Display	Jump in results display relative to X and Y, trigger positions from starting position.
Capture Screen	Capture a mouse selectable screen area and save as a *.pcx file.
Zoom	Zoom the display around X and Y cursors, between X and Y cursors or Zoom around independently of cursors.

MNEMONICS

100 User Defined per file	May be saved for recall in a different application. Unlimited files may be generated and saved.
PCI-X / PCI Bus	Inverse decode of all PCI-X / PCI initiator and target termination.

EXERCISER

Bus Width	Up to 64 Bit
Bus Speed	
PCI-X	1KH to 133 MHz
PCI	1KH to 66 MHz
Output Voltage Swing	3.3 V
Link	To the Analyzer, Start after defined events, Start after external trigger

DATA BLOCK GENERATION

- Data block generation of W1, W0 or user patterns.
- 8, 16, 32 or 64 bit wide.
- Up to 128K deep.
- Multiple blocks of data in to a single file.
- May be generated in the GUI and saved as ASCII format.
- May be generated in a text editor and imported to the exerciser program.

MASTER MODE

- Read/Write to I/O, MEM or configuration registers.
- DMA transfers of up to 128K, real-time.
- Single execution, loop up to 65535 or indefinite.
- Insert user defined Wait states, unlimited, any location.
- Force Interrupts, Errors, Parity Errors.
- Perform special bus cycles.
- Test memory blocks.
- Read Modify Write memory.
- Execute programs with or without GNT# from arbiter.
- Several programs may be cascaded for on-the-fly execution.
- Respond to Retry and Abort.
- Perform Dual address cycle programs.
- PCI-X Split Completion.

TARGET MODE

Termination Type	Transfer data, Retry, Disconnect with or without data, Abort with or without data, Split Response.
Decode Address	User defined I/O, Memory Read, Write single address or range, special cycle etc.
DEVSEL Speed	Medium, Slow, Subtractive or Below Subtractive.

PCI-X/PCI LOCAL MEMORY **

Read/Write Memory	1 M Byte memory on board for random access read/write operation.
Memory Depth	1MB organized as 8 x 128 KByte locations.
Transactions	32/64 bit
DEVSEL Speed Assertion	Slow

Initial Latency 7 States

VOLTAGE CHECK

Voltages Monitored	VDD of TA800, +5V, +3.3V, +12V. +3.3 V _{AUX} , +3.3 V, +5V for the DUT.
Drop Measured	-5%
Indicator	Red LED

VOLTAGE REQUIREMENT

+5V @ 10 mA

+3.3V @ 3 Amps

+/-12V @ 50 mA for extender operation.

** Note

PCI-X local memory to be supported with SW version 4.3 and higher.